09/814,244

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PATENT
Attorney Docket No. 70803

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,798,257

Confirmation No. 2001

Issued: Sept. 28, 2004

Name of Patentee: David Roe

Patent Title: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CLOCK SIGNALS ON A CHIP USING A SECOND PLL LIBRARY CIRCUIT CONNECTED TO A BUFFERED REFERENCE CLOCK OUTPUT OF A FIRST PLL LIBRARY CIRCUIT

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on July 29, 2005.

Kirk D. Williams, Esq. 7/29/05

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PATENT OFFICE MISTAKE (37 C.F.R. § 1.322)

Attn: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

It is requested that a Certificate of Correction be issued to correct Office mistakes found the above-identified patent. Attached hereto is a Certificate of Correction which indicates the requested correction. For your convenience, also attached are copies of selected pages (a) from the issued patent with errors highlighted, (b) from the original application as filed March 21, 2001 and (c) Amendment D filed February 28, 2004, with the correct text/instructions.

In re US Patent No. 6,798,257

It is believed that there is no charge for this request because applicant or applicants were not responsible for such error, as will be apparent upon a comparison of the issued patent with the application as filed or amended. However, the Assistant Commissioner is hereby authorized to charge any fee that may be required to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: July 29, 2005

By _____ 7/29/05

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,798,257

DATED : Sept. 28, 2004

INVENTOR(S) : David Roe

It is certified that error(s) appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 4, line 21, replace "11-113" with -- 111-113 --

Col. 5, line 22, replace "including;" with -- including: --

Col. 6, line 18, replace "output" with -- output, --

Col. 6, line 20, replace "circuits:" with -- circuits; --

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PATENT NO. 6,798,257
No. of additional copies

⇨ NONE (0)

AUG 8 – 2005

ture and functionality taught herein are extensible to an unlimited number of computer and communications systems, devices and embodiments in keeping with the scope and spirit of the invention. Embodiments described herein include various elements and limitations, with no one element or limitation contemplated as being a critical element or limitation. Each of the claims individually recite an aspect of the invention in its entirety. Moreover, some embodiments described may include, but are not limited to, inter alia, systems, integrated circuit chips, embedded processors, ASICs, and methods. The embodiments described hereinafter embody various aspects and configurations within the scope and spirit of the invention.

Methods and apparatus are disclosed for providing multiple clock signals on a chip using a second phase-locked loop library circuit connected to a buffered reference clock output of a first PLL library circuit which may be used, inter alia, in a computer or communications system, such as a computer or communications device, packet switching system, router, other device, or component thereof. Known prior circuits would typically use multiple off-chip reference clock signals for those applications that require multiple reference clocks. Certain embodiments may be particularly useful for possibly providing a lower-cost solution when, for example, such a circuit provides the capability to maintain tight timing, without sacrificing input pins, or excessively loading the PC board's clock driver. Various embodiments of such circuits include an ASIC or those using any chip implementation technology or combinations of technologies, including but not limited to VLSI design and discrete components.

As used herein, the term "system" is used generically herein to describe any number of components, elements, sub-systems, devices, packet switch elements, packet switches, networks, computer and/or communication devices or mechanisms, or combinations of components thereof. The term "computer" is used generically herein to describe any number of computers, including, but not limited to personal computers, embedded processors, ASICs, chips, workstations, mainframes, etc. The term "device" is used generically herein to describe any type of mechanism, including a computer or system or component thereof. The terms "task" and "process" are used generically herein to describe any type of running program, including, but not limited to a computer process, task, thread, executing application, operating system, user process, device driver, native code, machine or other language, etc., and can be interactive and/or non-interactive, executing locally and/or remotely, executing in foreground and/or background, executing in the user and/or operating address spaces, a routine of a library and/or standalone application, and is not limited to any particular memory partitioning technique. The terms "network" and "communications mechanism" are used generically herein to describe one or more networks, communications mediums or communications systems, including, but not limited to the Internet, private or public telephone, cellular, wireless, satellite, cable, local area, metropolitan area and/or wide area networks, a cable, electrical connection, bus, etc., and internal communications mechanisms such as message passing, interprocess communications, shared memory, etc. The terms "first, ""second," etc. are typically used herein to denote different units (e.g., a first element, a second element). The use of these terms herein does not necessarily connote an ordering such as one unit or event occurring or coming before the another, but rather provides a mechanism to distinguish between particular units.

Circuit **200** illustrated in FIG. **2** illustrates one embodiment for providing multiple clock signals on a chip using a second phase-locked loop (PLL) library circuit connected to a buffered reference clock output of a first PLL library circuit. In at least one application, circuit **200** provides the capability to maintain tight timing, without sacrificing input pins, or excessively loading the PC board's clock driver. Circuit **200** may implemented as an ASIC or using any chip implementation technology or combinations of technologies, including but not limited to VLSI design and discrete components.

As shown in FIG. **2**, circuit **200** includes a pad **208** which receives the off-chip reference clock signal **207**, which is electrically coupled to REFCLK input **109** of library circuit or macro **100**. First PLL circuit **100** provides a first set of one or more phase-locked loop clock outputs **101–103** and a buffered reference clock output **105**. BUFREFCLK output **105** is electrically coupled via link **210** to REFCLK input **119** of library circuit or macro **110**, which in turn provides a second set of one or more phase-locked loop clock outputs **111–113**.

111-113

In the past, typically multiple off-chip reference clock signals would have been used to in those applications that require multiple reference clocks. However, the embodiment illustrated by circuit **200** may be particularly useful for possibly providing a lower-cost solution when one PLL requires tight timing with the reference clock to produce one or more clock signals **201–203**, while the other PLL simply needs a clock to reference a frequency to produce one or more clock signals **211–213**. Moreover, embodiments are not limited to any particular library circuits or macros. Rather, the invention is extensible to an unlimited number of circuits, including, but not limited to the library circuits and macros disclosed herein.

FIG. **3A** illustrates one embodiment of a process for designing a circuit for generating a first and a second clock reference signals. Processing begins at process block **300**, and proceeds to process block **302** wherein a first phase-locked loop macro including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, and a buffered reference clock output is selected. Next, in process block **304**, a second phase-locked loop macro including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs is selected. Next, in process block **306**, the buffered reference clock output of the first phase-locked loop macro is connected to the on-chip reference clock input of the second phase-locked loop macro. In one embodiment, the circuit is included in an application-specific integrated circuit (ASIC). In one embodiment, the first phase-locked loop macro includes a buffer connected between the off-chip reference clock input and the buffered reference clock output. In one embodiment, the buffer is a non-inverting buffer, while in one embodiment the buffer is an inverting buffer.

FIG. **3B** illustrates one embodiment of a process for generating a first and a second internal clock reference signals on a chip. Processing begins at process block **320**, and proceeds to process block **322**, wherein a first phase-locked loop circuit receives an off-chip clock signal. In process block **324**, the first phase-locked loop circuit generates a buffered reference clock signal and the first set of internal clock reference signals. In process block **326**, a second phase-locked loop circuit receives the buffered reference clock signal. In process block **328**, the second phase-locked loop circuit generates the second set of internal clock reference signals. In one embodiment, the chip includes an application-specific integrated circuit (ASIC). In

one embodiment, the buffered reference clock signal input is a non-inverted representation of the received off-chip clock signal, while in one embodiment, the buffered reference clock signal input is an inverted representation of the received off-chip clock signal.

In view of the many possible embodiments to which the principles of our invention may be applied, it will be appreciated that the embodiments and aspects thereof described herein with respect to the drawings/figures are only illustrative and should not be taken as limiting the scope of the invention. For example and as would be apparent to one skilled in the art, many of the process block operations can be re-ordered to be performed before, after, or substantially concurrent with other operations. Also, many different forms of data structures could be used in various embodiments. The invention as described herein contemplates all such embodiments as may come within the scope of the following claims and equivalents thereof.

What is claimed is:

1. An application-specific integrated circuit (ASIC) comprising:

including:

- a first phase-locked loop circuit including; an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, a buffered reference clock output, and a buffer electrically connected to the off-chip reference clock input and the buffered reference clock output, and wherein the first phase-locked loop circuit is defined in one or more predefined libraries of circuits; and
- a second phase-locked loop circuit including: an on-chip reference clock input and a second set of one or more phase-locked loop clock outputs, wherein the second phase-locked loop circuit is defined in said one or more predefined libraries of circuits and is specified to be connected to an output of a receiver on the ASIC;
- wherein the buffered reference clock output of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit.

2. The ASIC of claim 1, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit includes at least two phase-locked loop clock outputs.

3. The ASIC of claim 1, wherein the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad of a chip.

4. An application-specific integrated circuit (ASIC) for receiving an external clock input to generate a first internal clock signal and a second internal clock signal, the ASIC comprising:

- a first phase-locked loop circuit means including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, a buffered reference clock output, and means for buffering a received off-chip reference clock signal electrically coupled to the off-chip reference clock input and the buffered reference clock output wherein the first phase-locked loop circuit means is defined in one or more predefined libraries of circuits; and

output, circuits;

- a second phase-locked loop circuit means including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs, wherein the second phase-locked loop circuit means is defined in said one or more predefined libraries of circuits and is specified to be connected to an output of a receiver on the ASIC;
- wherein the buffered reference clock output of the first phase-locked loop circuit means is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit means.

5. The ASIC of claim 4, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit means includes at least two phase-locked loop clock outputs.

6. The ASIC of claim 4, wherein the off-chip reference clock input of the first phase-locked loop circuit means is directly electrically coupled to a pad of a chip.

* * * * *

From Patent Filed Mar. 21, 2001

library circuit or macro 110, which in turn provides a second set of one or more phase-locked loop clock outputs 111-113.

In the past, typically multiple off-chip reference clock signals would have been used to in those applications that require multiple reference clocks. However, the embodiment illustrated by circuit 200 may be particularly useful for possibly providing a lower-cost solution when one PLL requires tight timing with the reference clock to produce one or more clock signals 201-203, while the other PLL simply needs a clock to reference a frequency to produce one or more clock signals 211-213. Moreover, embodiments are not limited to any particular library circuits or macros. Rather, the invention is extensible to an unlimited number of circuits, including, but not limited to the library circuits and macros disclosed herein.

FIG. 3A illustrates one embodiment of a process for designing a circuit for generating a first and a second clock reference signals. Processing begins at process block 300, and proceeds to process block 302 wherein a first phase-locked loop macro including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, and a buffered reference clock output is selected. Next, in process block 304, a second phase-locked loop macro including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs is selected. Next, in process block 306, the buffered reference clock output of the first phase-locked loop macro is connected to the on-chip reference clock input of the second phase-locked loop macro. In one embodiment, the circuit is included in an application-specific integrated circuit (ASIC). In one embodiment, the first phase-locked loop macro includes a buffer

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DAVID GLEN ROE

Application No. 09/814,244

Confirmation No. 2001

Filed: March 21, 2001

Group Art Unit: 2816

Examiner: COX, CASSANDRA F

For: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CLOCK SIGNALS ON A CHIP USING A SECOND PLL LIBRARY CIRCUIT CONNECTED TO A BUFFERED REFERENCE CLOCK OUTPUT OF A FIRST PLL LIBRARY CIRCUIT

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Commissioner For Patents, PO Box 1450, Alexandria VA 22313-1450, or being facsimile transmitted to the USPTO, 703-872-9306 on February 28, 2004.

Kirk D. Williams, Esq. 2/28/2004

AMENDMENT D

Commissioner for Patents
Alexandria, VA 22313-1450

Dear Sir:

The Office action dated December 3, 2003, and the references cited have been fully considered. In response, please enter the following amendments and consider the following remarks. Reconsideration and/or further prosecution of the application is respectfully requested.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

Amendment to the Claims:

The listing of clams will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1 (currently amended): ~~A circuit~~ An application-specific integrated circuit (ASIC) comprising:

a first phase-locked loop circuit including: an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, ~~and~~ a buffered reference clock output, and a buffer electrically connected to the off-chip reference clock input and the buffered reference clock output, and wherein the first phase-locked loop circuit is defined in one or more predefined libraries of circuits; and

including:

a second phase-locked loop circuit including: an on-chip reference clock input and a second set of one or more phase-locked loop clock outputs, wherein the second phase-locked loop circuit is defined in said one or more predefined libraries of circuits and is specified to be connected to an output of a receiver on the ASIC;

wherein the buffered reference clock output of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit.

2 (currently amended): The ~~circuit~~ ASIC of claim 1, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit includes at least two phase-locked loop clock outputs.

3-7 (canceled)

8 (currently amended): The ~~circuit~~ ASIC of claim 1, wherein the off-chip reference clock input of the first phase-locked loop circuit is directly electrically coupled to a pad of a chip.

9 (currently amended): ~~A circuit~~ An application-specific integrated circuit (ASIC) for receiving an external clock input to generate a first internal clock signal and a second internal clock signal, the ~~circuit~~ ASIC comprising:

a first phase-locked loop circuit means including an off-chip reference clock input, a first set of one or more phase-locked loop clock outputs, a buffered reference clock output, and means for buffering a received off-chip reference clock signal electrically coupled ~~between~~ to the off-chip reference clock input and the buffered reference clock output, wherein the first phase-locked loop circuit means is defined in one or more predefined libraries of circuits; and

a second phase-locked loop circuit means including an on-chip reference clock input and a second set of one or more phase locked loop clock outputs, wherein the second phase-locked loop circuit means is defined in said one or more predefined libraries of circuits and is specified to be connected to an output of a receiver on the ASIC;

wherein the buffered reference clock output of the first phase-locked loop circuit means is electrically coupled to the on-chip reference clock input of the second phase-locked loop circuit means.

10 (currently amended): The ~~circuit~~ ASIC of claim 9, wherein the first set of one or more phase-locked loop clock outputs of the first phase-locked loop circuit means includes at least two phase-locked loop clock outputs.

11-13 (canceled)